HTN8G27P040P
40W, 2496 - 2690 MHz LDMOS Amplifier

Product datasheet

Description

The HTN8G27P040P is an unmatched discrete LDMOS Power Amplifier with 40W saturated output power covering frequency range from 2496 - 2690 MHz.

Features

- Operating Frequency Range: 2496 - 2690 MHz
- Operating Drain Voltage: +28V
- Saturation Output Power: 40W
- Power Average: 6.3W
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Efficiency: 49%@2600MHz, LTE
- Gain: 17.5dB@2600MHz, LTE

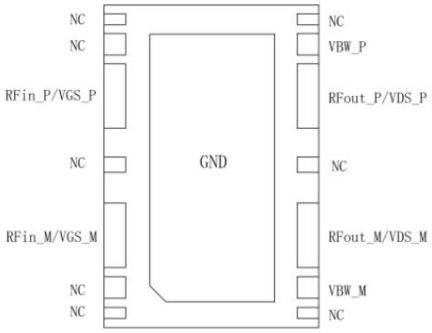
Applications

- 2.6 GHz mMIMO Final stage
- 2.6 GHz Driver stage

DFN 7.5x5 mm RoHS compliant

Dual-Flat No-Leads plastic Package

HTN8G27P040P



Note: Exposed backside of the package is the source terminal for the transistor

Pin Connections

Ordering Information

Part Number	Description
HTN8G27P040P	Reel Package
HTN8G27P040PEVB	2515 - 2675 MHz EVB

Typical Performance

RF Characteristics (LTE)

Freq (MHz)	Gain (dB)	Eff (%)	Pout (dBm)	ACPR (dBc)*
2600	17.5	49.0	38.0	-31.0

Test conditions unless otherwise noted: 25 °C, VDD = +30Vdc, IDQ= 120mA, PAVG = 38dBm (6.3W), FDD LTE 20MHz DL Signal, 10 dB PAR @ 0.01% CCDF test on WATECH Application Board

**Uncorrected DPD*

Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V_{DSS})	-0.5 to +65	V
Gate voltage (V_{GS})	-6 to +10	V
Drain voltage (V_{DD})	0 to +32	V
Storage Temperature (T_{STG})	-65 to +150	°C
Case Temperature (T_C)	-40 to +150	°C
Junction Temperature (T_J)	-40 to +225	°C

Electrical Specification

DC Characteristics (Main)

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=17uA	65	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vgs=Vds, Ids=17uA	-	1.5	-	V
Drain Leakage Current I_{DSS1}	Vgs=0V, Vds=65V	-	-	500	nA
Drain Leakage Current I_{DSS2}	Vgs=0V, Vds=28V	-	-	100	nA
Gate Leakage Current I_{GSS1}	Vgs=0V, Vds=10V	-	-	1	uA
Gate Leakage Current I_{GSS2}	Vgs=0V, Vds=-6V	-	-	200	uA

DC Characteristics (Carrier)

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	Vgs=0V, Ids=31uA	65	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	Vgs=Vds, Ids=31uA	1.3	-	1.7	V
Drain Leakage Current I_{DSS1}	Vgs=0V, Vds=65V	-	-	500	nA
Drain Leakage Current I_{DSS2}	Vgs=0V, Vds=28V	-	-	100	nA
Gate Leakage Current I_{GSS1}	Vgs=0V, Vds=10V	-	-	1	uA
Gate Leakage Current I_{GSS2}	Vgs=0V, Vds=-6V	-	-	200	uA

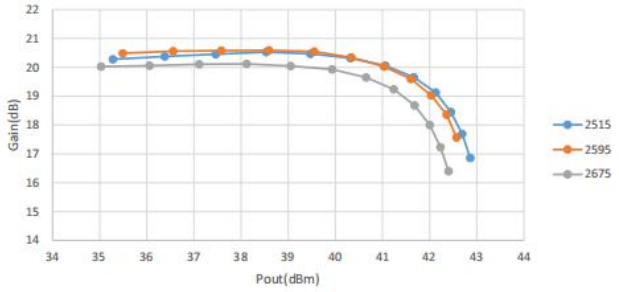
Load Mismatch Test

Condition	Test Result
VSWR=10:1, at all Phase Angles, VDD = +28Vdc, IDQ= 120mA, FDD LTE 20MHz DL Signal, 10 dB PAR @ 0.01% CCDF @2600 MHz test on WATECH Application Board	No Device Degradation

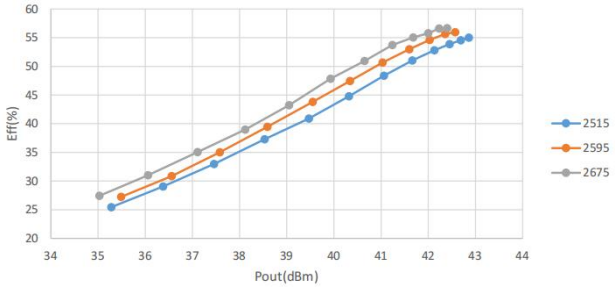
Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case (R_{TH})	T_{CASE}= 50°C, CW 40W	3.5	°C /W

Performance Plots 2515 - 2675 MHz Reference Design



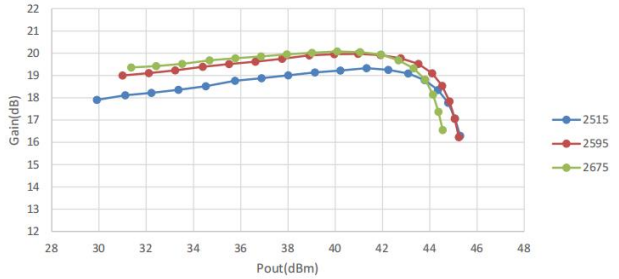
Pulsed CW, Gain vs Pout



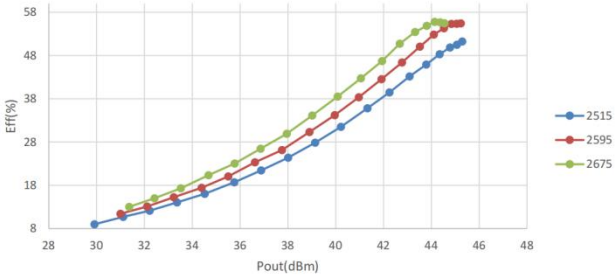
Pulsed CW, Efficiency vs Pout

Freq (MHz)	Gain (dB)	P1dB (dBm)	Eff(%)@P1dB	P3dB (dBm)	Eff(%)@P3dB
2515	20.53	41.77	51.45	42.72	54.64
2595	20.59	41.61	53.01	42.57	55.95
2675	20.12	41.33	54.02	42.26	56.60

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 120mA, PW = 1ms, DC= 10% test on WATECH Application Board



Pulsed CW, Gain vs Pout

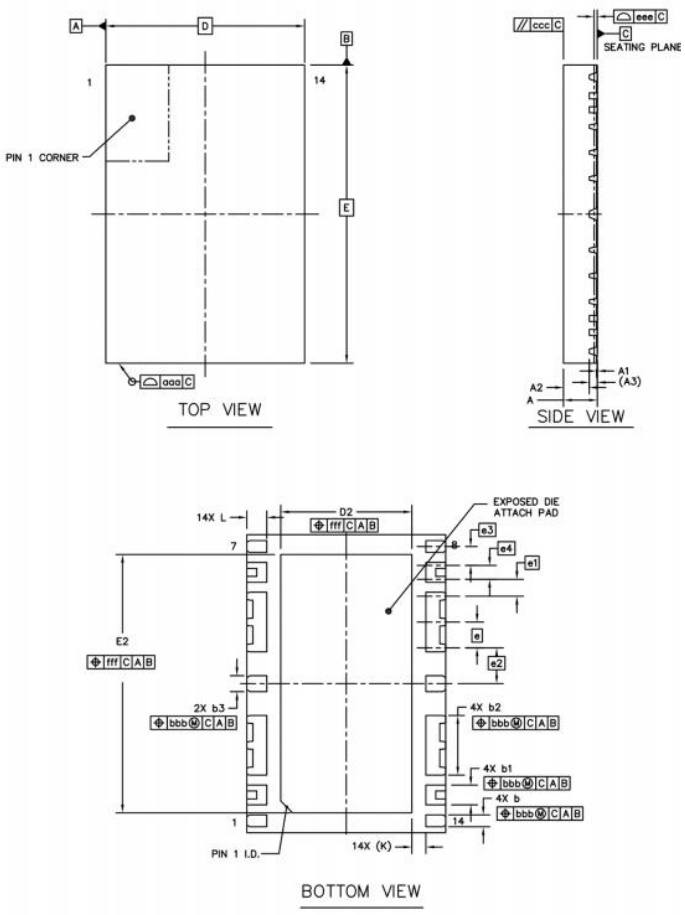


Pulsed CW, Efficiency vs Pout

Freq (MHz)	Gain (dB)	P1dB (dBm)	Eff(%)@P1dB	P3dB (dBm)	Eff(%)@P3dB
2515	19.33	44.37	48.38	45.28	51.23
2595	19.97	44.19	53.15	45.07	55.36
2675	20.08	43.55	54.10	44.44	55.58

Test conditions unless otherwise noted: 25 °C, VDD = +28Vdc, IDQ= 180mA, PW = 1ms, DC= 10% test on WATECH Application Board

Package Marking and Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.25	0.3	0.35
		b1	0.45	0.5	0.55
		b2	1.45	1.5	1.55
		b3	0.35	0.4	0.45
BODY SIZE	X	D		5 BSC	
	Y	E		7.5 BSC	
LEAD PITCH		e		0.65 BSC	
		e1		0.425 BSC	
		e2		0.9 BSC	
		e3		0.475 BSC	
		e4		0.35 BSC	
EP SIZE	X	D2	3.2	3.3	3.4
	Y	E2	6.4	6.5	6.6
LEAD LENGTH		L	0.4	0.5	0.6
LEAD TIP TO EXPOSED PAD EDGE		K		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Package Dimensions

Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114
ESD – Human Body Model (MM)	Class A	EIA/JESD22-A115
ESD – Charged Device Model (CDM)	Class III	JESD22-C101

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

Datasheet Status

Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

Abbreviations

Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

Revision history

Document ID	Datasheet Status	Release Date	Revision Version
Rev 1.0	Preliminary	April 2020	Preliminary
Rev 1.1	Preliminary	March 2023	New format based on English version datasheet
Rev 2.0	Product	April 2024	Product

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