

### Description

The HTH9G09P551S is an unmatched discrete LDMOS Power Amplifier with 550W saturated output power covering frequency range from 300 - 960 MHz.


### Features

- Operating Frequency Range: 300 - 960 MHz
- Operating Drain Voltage: 48V
- Saturation Output Power: 550W
- Excellent thermal stability due to low thermal resistance package
- Enhanced robustness design without device degradation
- Internally integrated enhanced ESD design

### Applications

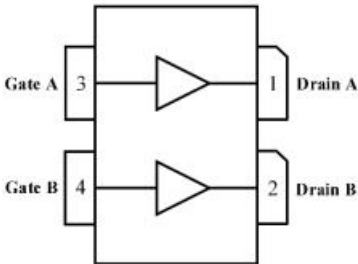
- Private network communication
- Amplifier for Micro and Macro Base Stations
- Repeaters/DAS
- Mobile Infrastructure
- 3GPP 5G NR FR1  
n5/8/12/13/14/18/20/26/28/29/67/85/100
- 4G-LTE  
B5/8/12/13/14/17/18/19/20/26/28/67/85/  
103





**ACS2110S-4L Air Cavity Splice**  
earless flanged package; 4 Leads  
**HTH9G09P551S**

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(Top View)

Note: Exposed backside of the package is the source terminal for the transistor

**Pin Connections**

### Ordering Information

Part Number	Description
HTH9G09P551S	Tray Package
HTH9G09P551S EVB	578-678 MHz EVB

### Typical Performance

#### RF Characteristics (CW, PW=100us, DC=10%)

Freq (MHz)	P5dB (dBm)	Gain (dB)	Eff (%)@49dBm	P5_Eff(%)	IRL(dB)
578	58.0	19.1	55.4	62.8	-10
628	58.1	19.8	53.3	60.2	-11
678	57.7	19.3	50.0	62.9	-12

Test conditions unless otherwise noted: 25 °C, VDD = 50Vdc, IDQ = 600mA, Vgsp=Vgsc-1.6V, Pout=49dBm, test on WATECH Application Board

#### RF Characteristics (WCDMA, PAR=9.9dB)

Freq (MHz)	Gain(dB)	Eff(%)	ACPR 5MHz(dBc)	ACPR 10MHz(dBc)	IRL (dB)
578	18.9	51.5	-29.3	-50.9	-11
628	19.6	49.8	-31.1	-51.4	-12
678	18.9	48.2	-33.0	-51.9	-12

Test conditions unless otherwise noted: 25 °C, VDD = 50Vdc, IDQ=600mA, Vgsp=Vgsc-1.6V, Pout=49dBm, test on WATECH Application Board

### Absolute Maximum Ratings

Parameter	Range/Value	Unit
Drain voltage (V <sub>DSS</sub> )	-0.5 to +120	V
Gate voltage (V <sub>GS</sub> )	-5 to +10	V
Storage Temperature (T <sub>STG</sub> )	-55 to +150	°C
Junction Temperature (T <sub>J</sub> )	-40 to +225	°C

### Electrical Specification

#### DC Characteristics (Carrier)

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage V <sub>(BR)DSS</sub>	Vgs=0V, Ids=156uA	115	-	-	V
Gate-Source Threshold Voltage V <sub>GS(th)</sub>	Vds=10V, Ids=156uA	2.2	2.7	3.1	V
Drain Leakage Current I <sub>DSS</sub>	Vds=110V, Vgs=0V	-	-	500	nA
Gate Leakage Current I <sub>GSS</sub>	Vds=0V, Vgs=10V	-	-	500	nA

### DC Characteristics (Peak)

Parameter	Conditions	Min	Typ	Max	Unit
Breakdown Voltage $V_{(BR)DSS}$	$V_{GS}=0V, I_{DS}=230\mu A$	115	-	-	V
Gate-Source Threshold Voltage $V_{GS(th)}$	$V_{DS}=10V, I_{DS}=230\mu A$	2.2	2.7	3.1	V
Drain Leakage Current $I_{DSS}$	$V_{DS}=110V, V_{GS}=0V$	-	-	500	nA
Gate Leakage Current $I_{GSS}$	$V_{DS}=0V, V_{GS}=10V$	-	-	500	nA

### Load Mismatch Test

Condition	Test Result
VSWR=10:1, at all Phase Angles, $V_{DD}=48V_{dc}$ , $I_{DQ}=400mA$ , $V_{GSP}=V_{GSC}-1.8V$ , $f=942.5MHz$ , WCDMA signal, $P_{out}=52dBm$ .	No Device Degradation

### Thermal Information

Parameter	Condition	Value (Typ)	Unit
Thermal Resistance Junction to Case ( $R_{TH}$ )	$f_{eq}=942.5MHz$ , $T_{case}=80C$ , WCDMA 1C, $P_{out}=49 dBm$	0.46	$^{\circ}C/W$

### Load Pull Performance Carrier

Test conditions unless otherwise noted: 25 °C,  $V_{DD} = 48V_{dc}$ ,  $I_{DQ} = 400mA$ ,  $PW = 100\mu s$ ,  $DC = 10\%$

Max Output Power-Carrier						
Freq (MHz)	$Z_{source} (\Omega)$	$Z_{load} [1] (\Omega)$	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	$1.0-j*5.0$	$2.2-j*0$	24.8	55.1	321	68.5
860	$2.1-j*8.0$	$1.9-j*0.3$	23.2	54.9	312	64.1
960	$7.2-j*14.7$	$1.7-j*0.5$	22.6	54.8	305	64.3

[1] Load impedance for optimum P3dB pout-Carrier

Max Drain Efficiency-Carrier						
Freq (MHz)	Z <sub>source</sub> (Ω)	Z <sub>load</sub> [2] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	1.0-j*5.0	2.1+j*1.5	26.6	53.7	234	77.3
860	2.1-j*8.0	1.5+j*1.1	25.5	53.3	215	74.8
960	7.2-j*14.7	1.7+j*0.5	24.5	53.9	240	72.2

[2] Load impedance for optimum P3dB efficiency-Carrier

### Load Pull Performance Peak

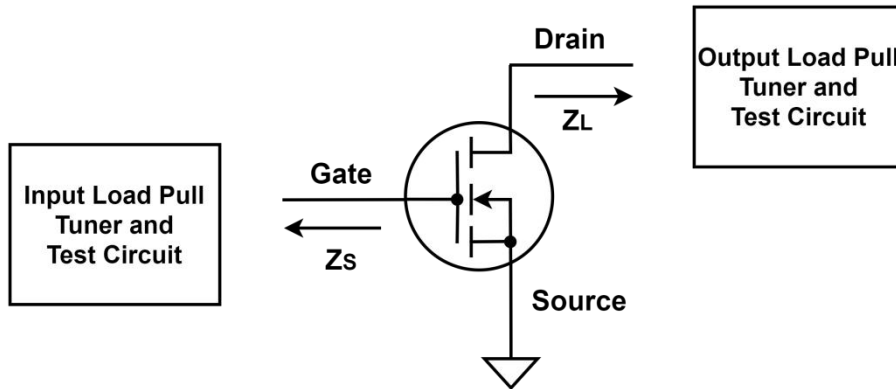
Test conditions unless otherwise noted: 25 °C, VDD = 48Vdc, IDQ= 500mA, PW = 100us, DC= 10%

Max Output Power-Peak						
Freq (MHz)	Z <sub>source</sub> (Ω)	Z <sub>load</sub> [3] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	1.1-j*5.2	1.4-j*0.5	24.3	56.8	482	67.5
860	2.0-j*8.5	1.4-j*1.0	22.6	56.7	468	62.2
960	7.5-j*16.0	1.5-j*0.9	21.5	56.9	485	63.6

[3] Load impedance for optimum P3dB pout-Peak

Max Drain Efficiency-Peak						
Freq (MHz)	Z <sub>source</sub> (Ω)	Z <sub>load</sub> [4] (Ω)	Gain (dB)	P3dB (dBm)	P3dB (W)	Eff (%)
760	1.1-j*5.2	1.2+j*0.5	26.1	55.1	321	75.2
860	2.0-j*8.5	1.2+j*0	24.6	55.6	363	72.5
960	7.5-j*16.0	1.2-j*0.2	23.7	55.4	347	68.8

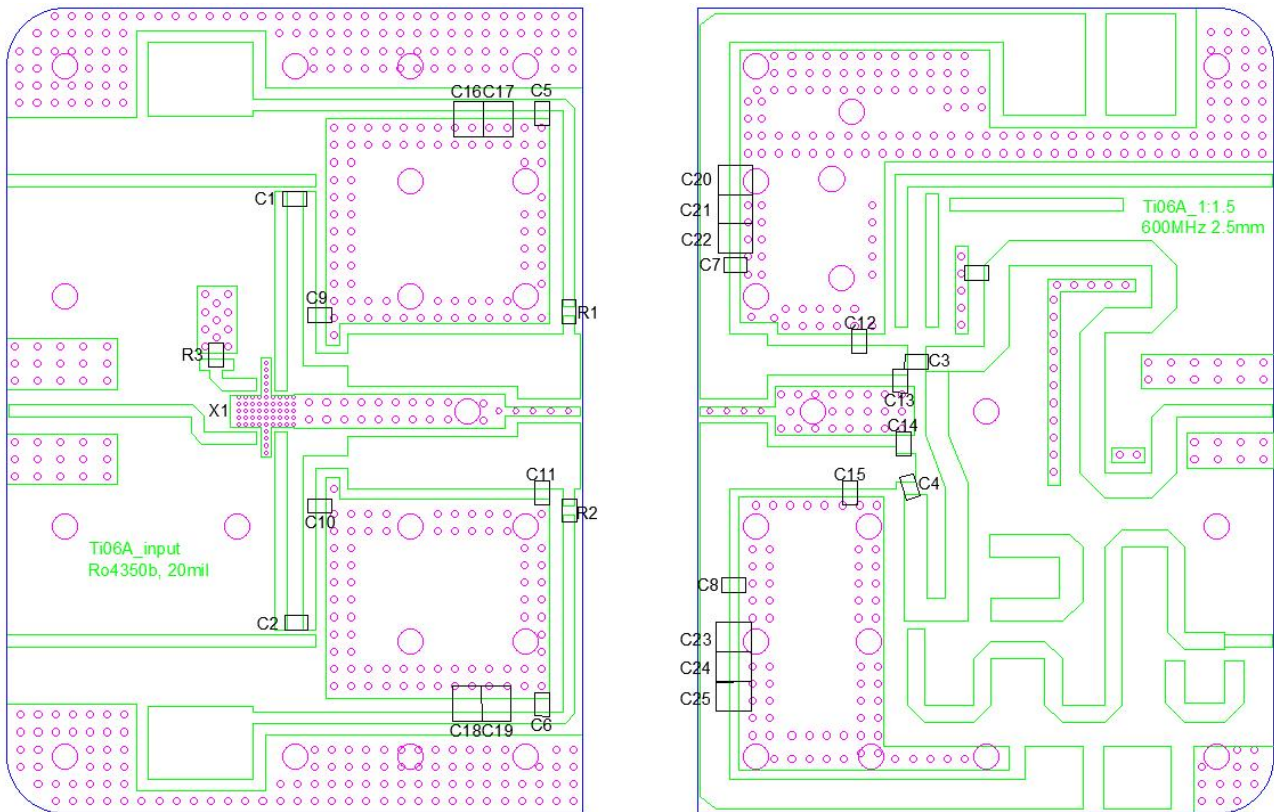
[4] Load impedance for optimum P3dB efficiency-Peak



$Z_{source}$  : Measured impedance presented to the input of the device at the package reference plane

$Z_{load}$  : Measured impedance presented to the output of the device at the package reference plane

### HTH9G09P551S 578-678MHz Reference Design

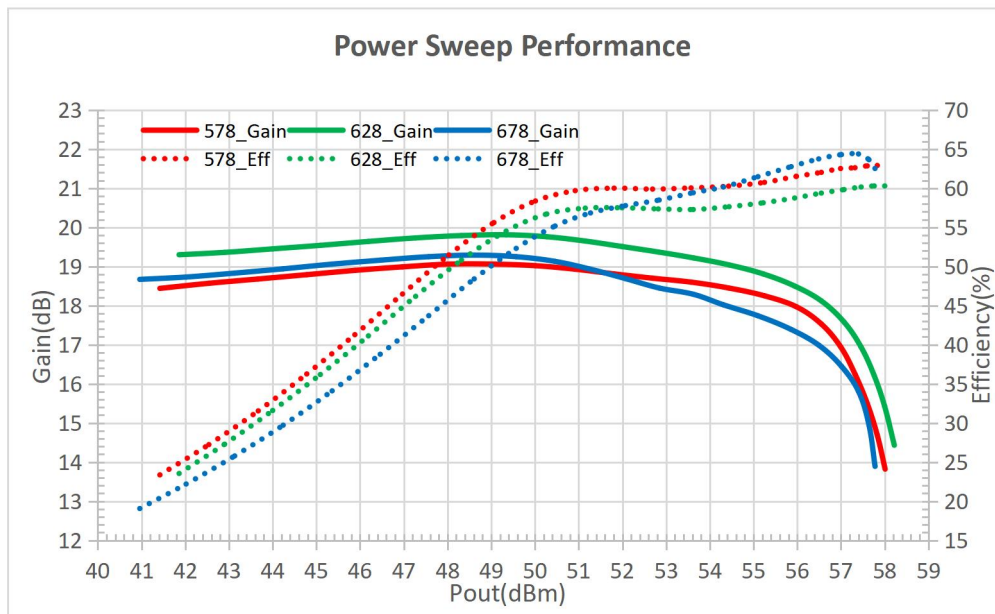


EVB Layout

### Bill of Materials (BoM) - HTH9G09P551S 578-678MHz Reference Design

Reference	Value	Description	Manufacturer	P/N
C1 - C8	150pF	0805 Chip Capacitor	Murata	GQM2195C2E151JB12
C9 - C10	9pF	0805 Chip Capacitor	Murata	GQM2195G2E9R0BB12
C11	24pF	0805 Chip Capacitor	Murata	GQM2195C2E240JB12
C12 - C13	9.1pF	0805 Chip Capacitor	Murata	GQM2195G2E9R1BB12
C14	13pF	0805 Chip Capacitor	Murata	GQM2195C2E130JB12
C15	18pF	0805 Chip Capacitor	Murata	GQM2195C2E180JB12
C16-C25	10uF	1210 Chip Capacitor	Murata	GRM32EC72A106KE05L
R1,R2	10 Ω	0805 Chip Resistor	SMD	
X1	3dB,90°	Hybrid Coupler	Anaren	X3C07F1-03S
R3	50 Ω ,25W	Load Resistor	Anaren	C16A50Z4
PCB	Rogers4350B,20mil thickness			

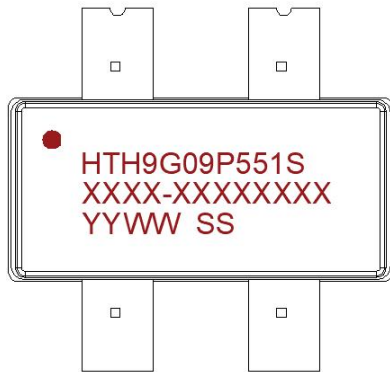
### Performance Plots



**Pulsed CW, Gain and Efficiency vs Pout**

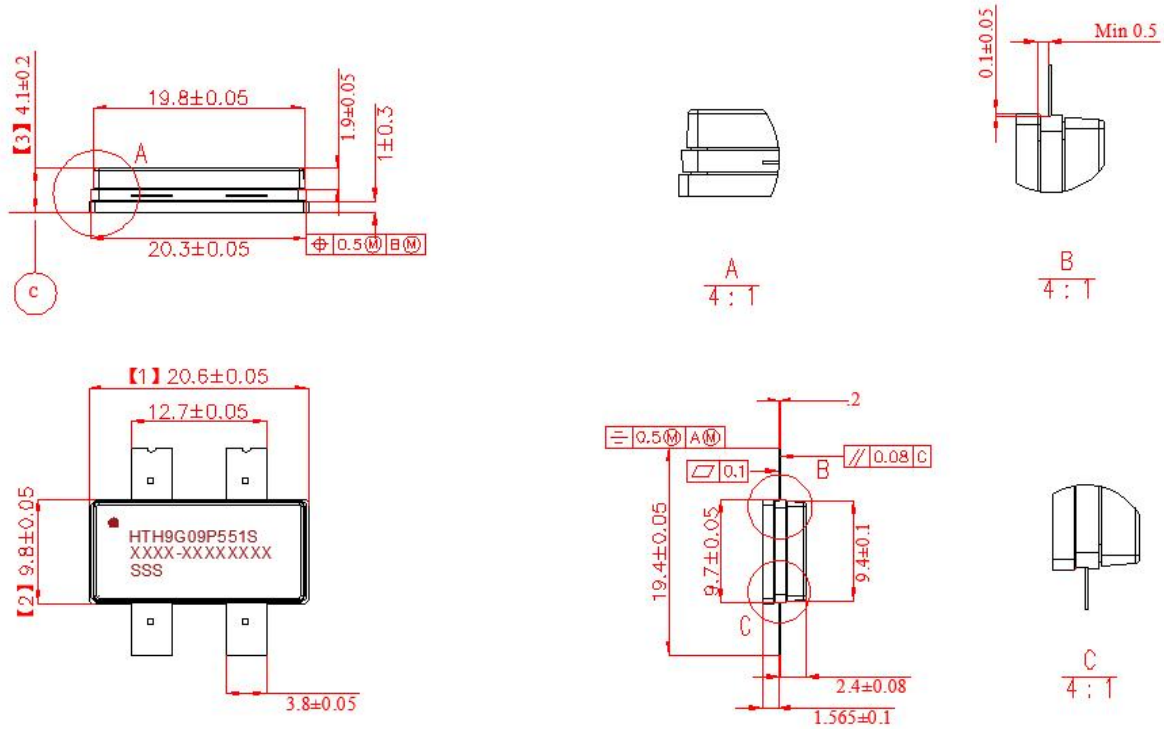
Test conditions unless otherwise noted: 25 °C, VDS = 50Vdc, IDQ= 600mA , Vpeak=2.1V, PW = 100us, DC= 10% test on WATECH Application Board

### Package Marking and Dimensions



- Line1 (fixed): Device name in W/O
  - Line2 (unfixed): Marking Lot No in W/O  
(Sample: E596-20140001)
  - Line3 (unfixed): Date Code + JY
- This Marking SPEC only stipulates the content of Marking. For marking requirements such as font and size, please refer to the latest version of "Watech Product Printing Specification"

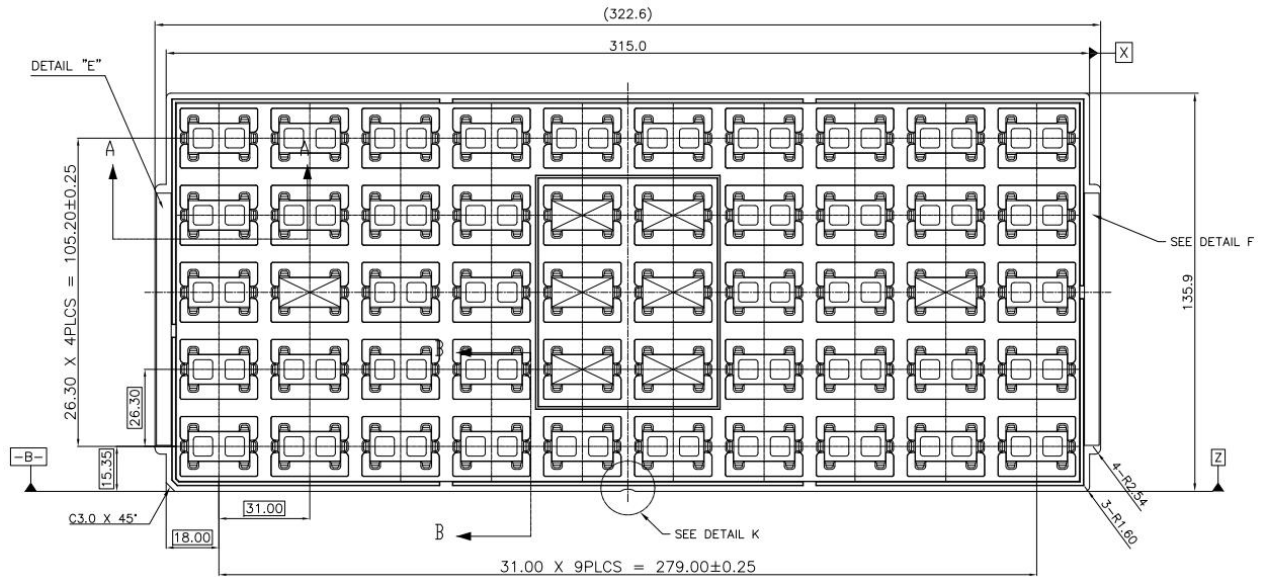
### Marking



### Package Dimensions

### Tape and Reel Information

Package Type	Qty/Tray(pcs)	Qty/Box(pcs)	Qty/Carton(pcs)
ACS2110S-4L	50	300	1800



### Tape & Reel Packaging Descriptions

### Handling Precautions

Parameter	Grade
Moisture Sensitivity Level MSL	3

Parameter	Rating	Standard	
ESD – Human Body Model (HBM)	Class 1B	JESD22-A114	
ESD – Me Model (MM)	Class A	EIA/JESD22-A115	
ESD – Charged Device Model (CDM)	Class III	JESD22-C101	

### RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.



## Datasheet Status

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Document status	Product status	Definition
Objective Datasheet	Design simulation	Product objective specification
Preliminary Datasheet	Customer sample	Engineering samples and first test results
Product Datasheet	Mass production	Final product specification

## Abbreviations

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Acronym	Definition
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
CW	Continuous Waveform

## Revision history

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Document ID	Datasheet Status	Release Date	Revision Version
Rev 1.0	Preliminary	Feb. 2023	Preliminary
Rev 1.1	Preliminary	Jul. 2023	New format based on English version datasheet
Rev 2.0	Product	Sep. 2023	Update load pull test result
Rev 2.1	Product	March 2024	Update packaging information



## Contact Information

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For the latest specifications, additional product information, worldwide sales and distribution locations and information about WATECH:

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